(32)

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॥ अंतरी पेटवू ज्ञानज्योत ॥

North Maharashtra University, Jalgaon

Syllabus for Third Year Engineering Degree Course in

COMPUTER ENGINEERING

(w.e.f. July, 2000)

North Maharashtra University, Jalgaon

T.E. (Computer Engineering)

(With effect from July, 2000)

Term I

Sr. No.	Subject Code	Subject	Teaching Scheme Hours / Week		Examination Scheme				
			Lectures	Practical	Paper duration Hours	Maximum Marks			
						Paper	Termwork	Practical	Oral
1		Theory Of Computer Science	4	--	3	100	25	--	--
2		Microprocessor Systems	4	4	3	100	25	25	--
3		Digital Systems Design	4	4	3	100	25	25	--
4		Signals and Systems	4	--	3	100	25	--	--
5		Numerical Computation and Programming	4	2	3	100	25	25	--
		Total	20	10	--	500	125	75	--
		Grand Total	30		--	700			

Term II

Sr. No.	Subject Code	Subject	Teaching Scheme Hours / Week		Examination Scheme				
			Lectures	Practical	Paper duration Hours	Maximum Marks			
						Paper	Termwork	Practical	Oral
1		Data Communication	4	2	3	100	25	25	--
2		Computer Organization	4	--	3	100	--	--	--
3		Language Processors	4	2	3	100	25	--	--
4		Computer Peripherals and Interfacing.	4	4	3	100	25	25	--
5		Instrumentation and Diagnostic Tools	4	2	3	100	25	25	--
6		Practical Training / Special Study/ Minor Project	--	--	--	--	25	--	--
		Total	20	10	--	500	125	75	--
		Grand Total	30		--	700			

Total Marks of Term I + Term II = 1400 Marks

Term I Paper 1
Theory Of Computer Science

Teaching Scheme
Lectures 4 Hrs./Week

Examination Scheme:
Theory Paper : 100 Marks
(3 Hrs. duration)
Termwork : 25 Marks

Unit 1

Mathematical preliminaries, alphabets, string, language states, graphs and trees. Concept Of basic machine, finite state machine (FSM), finite state model, FSM examples, adjacency matrix, Moore and Mealy FSM's, deterministic and non-deterministic FSM's,state equivalence machine, state minimization of FSM.

20 Marks (10 Hrs)

Unit 2

Properties of regular sets, alphabets, words, regular sets and regular expressions, closed regular sets and pumping lemma , FSM - associated transition graphs and regular expression, decision algorithms for regular sets, FSM properties and limitations 20 marks (10 Hrs.)

Unit 3

Turing machine (TM), an introduction, definitions, formulation of TM model, power of TM over FSM, TM examples, Universal TM (UTM), Church's Turing Hypothesis, multistack machines, TM limitations, halting problem, incompleteness and undecidability. 20 marks (10 Hrs.)

Unit 4

Production Systems, post canonical system, acceptors and generators, Markov algorithms. Grammars, rules, formulization, ambiguity, reduced form, derivation trees, Chomsky hierarchy derivation graphs, context free grammar, simplification of context free grammar, existence of inherently ambiguous context free languages. 20 marks (10 Hrs.)

Unit 5

Push down stack memory machine (PDM), definitions, PDM examples, power of PDM, deterministic and non- deterministic PDM'S, push down automata and context free language properties of context free languages.
Functions - Introduction, total and partial recursive functions. 20 marks (10 Hrs)

References :

1 Theory of Computer Science, E V. Krishnamurthy, Wiley - Eastern Publication.
2 Introduction to automata theory, languages and computation, Hoproft, Ullman, Naroea Publication.

Term I Paper 2
Microprocessor Systems.

Teaching Scheme
Lectures 4 Hrs./Week
Practicals : 4 Hrs./Week

Examination Scheme :
Theory Paper : 100 Marks.
(3 Hrs. duration)
Termwork : 25 Marks
Practical : 25 Marks

Unit 1

8086 CPU architecture, 8088 architecture, programming module, segmented memory, addressing modes, instruction sets. 20 marks (10 Hrs)

Unit 2

BIOS and DOS . Introduction to DOS, structure of DOS, assembly language programming in MSDOS using BIOS and DOS interrupts. Microprocessor programming techniques,time delay loops, procedures and macros. 20 marks (10 Hrs.)

Unit 3

8086 Configurations : Basic 8086 configuration, minimum and maximum modes, system bus timing, interrupt priority management, programmable interrupt controller (PIC) 8259A. 20 marks (10 Hrs)

Unit 4

Main memory design : 8086 CPU Read/Write timing, SRAM and ROM interfacing requirements, address decoding techniques - full partial, block, PROM. Troubleshooting the memory module. 20 marks (10 Hrs)

Unit 5

Multiprocessor Configuration . Queue status and locked facility, 8086 based multiprocessor system, co-processor configuration, closely coupled configurations. Overview of loosely coupled configuration, 8087 NDP, 8087 data types and processor architechture. 20 marks (10 Hrs)

References

1. The 8086/ 8088 family ; Design, programming and Interfacing, John E. Uffenbeck, Prentice-Hall of India Ltd.
2. Microcomputer System : The 8086/8088 family architecture, programming and design, Yucheng Liu and Glenn A Gibson, Prentice-Hall of India Ltd.
3. Assembly language programming, Allen Watt.
4. Assembly Language Programming, Peter Able , Prentice - Hall of India Ltd.
5. Microprocessor and Interfacing : Programming and Hardware, D.V. Hall, Tata Mc-Graw Hill.
6. The Intel Micrprocessor 8086, 80186,80286, 80386 and 80486 Architecture, Programming and Interfacing, Barry Brey, Prentice-Hall of India Ltd.

List of Experiments :

8086 assembly language programming

Group A

1. Addition of two numbers, inputs from keyboard.
2. String display.
3. BCD to HEX conversion.
4. HEX to BCD conversion.
5. Program using Near procedure.
6. Program using Far procedure.
7. Array sorting using bubble sort.
8. Program using 8087 instruction set.

Group B

9. Program using exchange sort.
10. Program using macros.
11. Program for password.
12. Programm using 8087 instruction set.
13. Program using structures.
14. Memory to memory block transfer.
15. Study of BIOS and DOS interrupts.
16. Study of MASM directories.

The termwork should include a minimum of twelve experiments, six each from groups A and B. The termwork marks will be based on performance in theory and practicals, having a weightage of 40% and 60% respectively.

Term I Paper 3
Digital Systems Design

Teaching scheme :
Lectures : 4 Hrs/week
Practicals : 4 Hrs/week

Examination scheme :
Theory paper : 100 Marks
(3 Hrs duration)
Termwork : 25 Marks
Practical :25 Marks

Unit 1

Basic principles in digital systems design:Clock , Noise, assumptions, races, hazards, digital systems and components. Combinational Logic Design :Design using multiplexers, demultiplexers, decoders, encoders and code converters. 20 marks (10 Hrs)

Unit 2

ROM and PLD Design : Basic structure of read only memory, size of ROM and design using ROM. Structure of programmable logic arrays and array logic, design using PLA, FPLA and PAL. Design using random access memory, memory decoding. 20 marks (10 Hrs)

Unit 3

Sequential logic design . Analysis of clocked sequential circuit, state reduction and assignment. Design procedure and design of registers, shift registers, ripple counters, synchronous counters, Sequence generators and detectors.

20 marks (10 Hrs.)

Unit 4

Asynchronous sequential logic Design : Analysis procedure, circuits with latches, design procedures. Reduction of state and flow tables, race-free state assignment, hazards, design examples. 20 marks (10 Hrs)

Unit 5

Algorithmic State machines . ASM chart definition, standard symbols for ASM charts. Methods of implementing an ASM chart by using Tradiational method, MUX - controller, ROM- controller,and One - HOT controller. Generation of ASM chart for different waveforms. Miscellaneous problems of ASM charts such as traffic light, washing machine, vending machine, etc. 20 marks (10 Hrs)

References :

1 Digital design, 2 nd edition, M Morris Mano, Prentice - Hall of India Ltd.

2. Digital Electronics circuits and systems, V.K. Puri, Tata McGraw - Hill.

3. Digital logic and Microprocessor, Fredrick J. Hill and G.R. Peterson, John Wiley and Sons.

List of experiments :

Group A

1 Simplification of Boolean function.(This experiment should demonstrate the relationship betweer a boolear fuction and corresponding logic diagram)

2. Combinational logic design. (In this experiment design, construct and test four combinational logic circuits)

3 Gray to binary code converter. 4. BCD to nine's complementer.

5 BCD to seven segment display converter. 6. Binary and decimal number counter.

7 Design with multiplexer IC 74151.

8. Design, construct and test a half adder circuit with the help of one Ex-OR and two NAND gates.

Group B

1 Design, construct and test a full adder with the help of two half adders and one OR gate.

2 Design adder/subtractor circuit using IC 7483.

3. Design comparator circuit.

4. Construct, test and investigate the operation of various flip-flop circuits.

5 Design two - bit/ three - bit up - down counter using J-K flip-flop.

6 Design ripple/decimal counter using IC 7473 and IC 7408.

7 Design ring counter using the IC 7495.

8 Construct and test a sequence generator and detector circuit.

The termwork should include a minimum of twelve experiments, six each from groups A and B. The termwork marks will be based on performance in theory and practicals having a weightage of 40% and 60% respectively.

Term I Paper 4

Signals and Systems

Teaching scheme .

Lectures : 4 Hrs/week

Examination scheme :

Theory paper : 100 Marks

(3 Hrs duration)

Termwork : 25 Marks

Unit 1

Fourier analysis, Laplace transform, Z - Transform, sampling, representation of continuous time signals by its samples, sampling theorem, reconstruction of signals from its samples using interpolation, aliasing, discrete time processing of continuous time signals. 20 marks (10 Hrs)

Unit 2

Transfer fuction, signal flow graph : Block reduction techniques, analysis of steady state error (type 0,1 ,2 systems), characteristics of second order system , time response, frequency response. 20 marks (10 Hrs)

Unit 3
Stability and dynamic response : Characteristic equation, the Routh criterion, Cauchy's principles of argument and Nyquist criterion. Relative stability, gain and phase margins, closed loop frequency response. 20 marks (10 Hrs)

Unit 4
Frequency response analysis : Bode diagram - magnitude versus frequency, phase versus frequency, system stability analysis from Bode diagram , system transient analysis from Bode diagram, root locus analysis. 20 marks (10 Hrs)

Unit 5
Digital and sampled data control : Sampling process, feedback system analysis in Z domain. State space analysis, state variable concept, state variable modelling, transformation of state variables, state diagram. 20 marks (10 Hrs)

References :

1. Signals and systems, Openheim, Prentice - Hall of India Ltd.
2. Automatic Control system, Thater, Jaico Publication.
3. Digital Control system, M. Gopal.
4. Digital Control and State Variable method, M.Ropa.

Term I Paper 5

Numerical Computation and Programming

Teaching scheme :
Lectures : 4 Hrs/week
Practical : 2 Hrs/week

Examination scheme :
Theory paper : 100 Marks
(3 Hrs duration)
Termwork : 25 Marks
Practical : 25 Marks

Unit 1
Linear System of equations : Direct methods - matrix inversion, Gauss elimination - partial and complete, Gauss - Jordan elimination, triangularization, iterative method- Jacobi iteration, Gauss Siedal. 20 marks (10 Hrs)

Unit 2
Solution of ordinary differential equation : Euler method - one step and multistep, modification and improvement of Euler's method, Heun's method, improved polygon method, Taylor series, Runge Kutta method - 2nd, 3rd, 4th order. 20 marks (10 Hrs)

Unit 3
Transcendental and polynominal equation : Initial approximation, intermediate value theorem, bracketing methods - bisection, false position theorem, iteration methods based on first degree equation, secant, newton - raphson methods. 20 marks (10 Hrs)

Unit 4
Interpolation by approximation : Polynomial approximation by Taylor's series, lagrange's and Newton's method - two point or second order - linear, Aitken Newton's divided difference, finite difference operators, relation between them, Greogory - Newton forward and backward, stirling's central difference, least square - 1st, 2nd degree. 20 marks (10 Hrs)

Unit 5
Numerical Integration : by interpolation - Newton cotes, trapezoidal, Simpson's 1/3 and 3/8, by undeterminent coefficient- Gauss, Legendre, Lobatto. 20 marks (10 Hrs)

References :

1. Numerical Methods for scientific and engineering computation, 3rd edition, M.K. Jain, Iyengar, New Age International.
2. Computer oriented numerical methods, Rajaraman.
3. Numerical methods for engineers, Steven Chapra.
4. Numerical methods, E Balaguruswamy, Tata McGraw Hill .

List of Experiments :

1 and 2 : Evaluation of unknowns of linear equation using two methods.
3 and 4 : Solution of ordinary differential equation using any two methods.
5, 6 and 7 : Finding the roots of equations using any three methods.

8 and 9 : Evaluation of interpolating polynomial and fitting of curve by any two methods.
10,11 and 12 : Integration by interpolation and undeterminant coefficient by any three methods.
The termwork should include a minimum of eight experiments from the above list .The termwork marks will be based on performance in theory and practicals with weightage of 40% and 60% respectively.

Term II Paper I

Data Communication

Teaching scheme :
Lectures 4 Hrs/week
Practicals : 2 Hrs/week

Examination scheme:
Theory paper : 100 Marks
(3 Hrs duration)
Termwork : 25 Marks
Practical : 25 Marks

Unit 1
Basic Concepts : Introduction to communication, uses of communication, structure and types of communication systems. Communication channels, characteristics of communication channels. Electromagnetic waves, frequency and wavelength, bandwidth and channel capacity. Modulation, types of modulation, frequency, amplitude and phase modulation.
20 marks (10 Hrs)

Unit 2
Multiplexing : space - division multiplexing, frequency division multiplexing, time - division multiplexing, Multiplexers and concentrators Telephone system and modem : Basic telephone, Telephone office function, dialling, pulse and tone dialling telephone lines. Modems, role of modem, modem functions, operation of modem, originate and answer modem, four wire modem.Bell 103, 212 and 202 modem.
20 marks (10 Hrs)

Unit 3
Networks Computer networks and distributed system, network criteria, applications, protocols.
Protocols : Command response, token passing, interrupt-driven and CSMA/CD.
Topology : Mesh, star, tree, bus, ring and hybrid topologies. Network categories: LAN, MAN , WAN ,and inter- networks.
20 marks (10 Hrs)

Unit 4
ISO-OSI model . Basic architecture, structure of ISO-OSI model, layers, protocols and interface.Encoding : Analog to digital, pulse amplitude modulation (PAM) , pulse code modulation (PCM). Digital to analog, amplitude shift keying (ASK), frequency-shift keying (FSK), phase shift keying (PSK),quadrature amplitude modulation (QAM),DTE-DCE interface, RS-232C, X.21 standard.
20 marks (10 Hrs)

Unit 5
Error detection and correction : Types of errors, detection techniques, VRC, and CRC error correction, Hamming code, Switching, circuit, packet,message switching, ISDN, services, history, subscriber access to the ISDN,ISDN layers. X.25 layers and structure HDLC/SDLC protocol.
20 marks (10 Hrs)

References :

1. Data communications,William L. Schweber, McGraw - Hill International Edition.
2. Introduction to Data communications and networking Behrouz Forouzan, WCB/McGraw-Hill.
3. Computer Networks, Andrew S.Tannenbaum, Prentice Hall of India .

List of Experiments :

1. PC to PC communication
2. Implement simplex system.
3. Implement half duplex/full duplex system.
4. Implement stop and wait protocol.
5. Implement go back 'N' protocol.
6. Implement single bit sliding window protocol.

The termwork should include minimum of five experiments from the above list.The termwork marks will be based on performance in theory and practicals with weightage of 40% and 60% respectively.

Term II Paper 2

Computer Organization

Teaching scheme :
Lectures : 4 Hrs/week

Examination scheme:
Theory paper : 100 Marks
(3 Hrs duration)

Unit 1
Introduction to system concepts : Computer operating cycles, instruction formats for larger machines, fixed and expanding opcodes, zero, two and three address schemes. Processor organization : instruction set design, design exercise of ALU , 68000 architecture,normal and exceptional processing. 20 marks (10 Hrs)

Unit 2
Information representation, data types, fixed and floating point representation, IEEE format for floating point, fixed point and decimal algorithm, Booth's algorithm, algorithms for floating point operations (assembly / C language suggested for programs. 20 marks (10 Hrs)

Unit 3
Control unit design, hardwired control design methods and implementation, micro-programmed control concepts and control design considerations, bit - slice architecture, 2900 family CPU design, emulation. 20 marks (10 Hrs)

Unit 4
Memory organization : memory hierarchies, Cache memories organization, virtual memory and implementation, performance considerations Content addressable memories, extended memories, memory management in 68000 family cache design. 20 marks (10 Hrs)

Unit 5
System Organization : buses, interconnection system bus, CPU and IO bus - bus operation, UNIBUS, Multibus, IEEE 488 I/O addressing data transfer synchronization,I/O interfaces,I/O channels, SCSI bus. RISC architecture : Concepts, CISC versus RISC, Advantages of RISC. 20 marks (10 Hrs)

References :

1. Computer organization, 4th edition, Hamacher, Vranesic,Zaky, Mc-Graw Hill International.
2. Computer Architecture and Organization , 2nd edition Hayes, McGraw Hill International edition.
3. Structured Computer Organization, Tannenbaum, Prentice - Hall of India.

Term II Paper 3

Language Processors

Teaching scheme :
Lectures : 4 Hrs/week
Practical : 2 Hrs/week

Examination scheme:
Theory paper : 100 Marks
(3 Hrs duration)
Termwork : 25 Marks

Unit 1
Introduction to system programming, types of s/w and application software, system programming and system programs, need of system software, assemblers, loaders, compilers, interpreters, macros, operating systems and formal systems, translators and its types.Programming languages, overview of machine languages. Assembly languages and high level languages,overview of assembly process, comparison of H.L.L.,assembly and machine languages. Importance and features of high level languages, H.L.L. - datatypes, data structures, allocation and storage , block structured programming language and its scope, rules. 20 marks (10 Hrs)

Unit 2
Detailed study of assemblers : Structure of assembler, basic functions, machine dependent and machine independent feature of assembler, type of assemblers i.e single pass, multipass, cross assembler, design option of assembler, general design procedure of assembler,design of pass - I and pass - II assembler (with reference to 8086 assembler), single pass assembler for IBM PC, Implementation examples - MASM example. Macros and macro processor- definition of macros, functions of macro processor, features of macro facility, design option of macro - processor, i.e. single pass and 2 pass macroprocessor, detailed design of two pass macroprocessor. 20 marks (10 Hrs)

Unit 3
Grammer and scanner, overview of compilation, process, programming language grammer, derivation, reduction and syntax tree, ambiguity, regular grammer and regular expression. Basic function of compilers, machine dependent machine independent features of compilers. Types of compilers, single pass, multipass, cross compiler and pseudocode compiler. Phase of compiler, lexical phase, syntax phase and semantics phase, interpretation, optimization storage assignment, code generation. 20 marks (10 Hrs)

Unit 4
Scanning and parsing - functions of parser, parsing techniques, top down and bottom up parsing. Limitations of top-down parser, shift reduce and recursive descent parser, operator precedence parser, predictive parser, L-R parsers syntax directed translation, symbol table organization and memory allocation,elementary symbol table organization, hash tables, linked list and tree structured symbol tables, memory allocation, static and dynamic memory allocation.
20 marks (10 Hrs)

Unit 5
Loaders and linkage editors - basic loader functions, relocation and linking concept various loading schemes with their advantages and disadvantages, linking methods, design of a direct linking loader, specification of problem, specification of data structures format of databases, algorithms, a linker for MS-DOS, software development tools . software tools for program development YACC, LEX tools for programming testing, text editors - various types of text editors, structure of editors, function of editors, tools for debugging, debug monitors MS debug for program testing.
20 marks (10 Hrs)

References :

1 System programming , John Donovan, Tata McGraw Hill
2. System Programming and operating systems,D.M. Dhamdhere, Tata McGraw - Hill.
3 System Software and introduction to system programming, Lenard L.Beck, Addison Wiley publication

List of Experiments :

1 Assembler design (for hypothetical system)
2 Simple macro-preprocessor.
3. Recursive descent parser.
4. Lexical analysis.
5 Simple text editor.
6. Design of simple loader.

The termwork will include a minimum of five experiments from the above list. The termwork marks will be based on performance in theory and practicals with the weightage of 40% and 60% respectively.

Term II Paper 4

Computer Peripherals and Interfacing.

Teaching scheme
Lectures . 4 Hrs/week
Practical 4 Hrs/week

Examination scheme:
Theory paper . 100 Marks
(3 Hrs duration)
Termwork : 25 Marks
Practical : 25 Marks

Unit 1
Methods of parallel data transfer 8255 programmable peripheral interface (PPI), parallel printer interfacing - centronics interface standard, keyboard interfacing, interfacing LED displays, keyboard and display interfacing using 8279, 8253 programmable interval timer
20 marks (10 Hrs)

Unit 2
Stepper motor interfacing ,DAC operation, characteristics, specifications and interfacing, ADC specifications and interfacing, direct memory access, 8237 DMA controller, serial communication asynchronous,synchronous,RS- 232C, BISYNC., HDLC and SDLC protocols, 8251 USART.
20 marks (10 Hrs)

Unit 3
BIOS and DOS interrupt services - CRT output keyboard input , DOS disk file system, DOS boot record, FAT ,DOS disk services,DOS files and file management, hard disk format,device drivers, installable device drivers, structure of device driver
20 marks (10 Hrs)

Unit 4

Hardware organization of PC, PC family, motherboard components,logic , I/O channel, memory map, I/O map, Interrupts, DMA channels, keyboard, keyboard interface block diagram, parallel interface , serial interface, serial port, real time clock (RTC), PC add on cards. 20 marks (10 Hrs)

Unit 5

Disk recording methods - FM, MFM, floppy disk controller (FDC) logic, FDC block diagram, hard disk controller (HDC) logic, HDC block diagram, CRT display , CRT controller principle,PC display adapters, monochrome display adapter (MDA), color/graphics adapter (CGA), VGA, SVGA principle of AGP. 20 marks (10 Hrs)

References :

1. Microprocessors and interfacing : programming and hardware, Douglas V. Hall, Tata McGRaw - Hill.
2. The 8086 microprocessor : Programming and Interfacing the PC, Kenneth J. Ayala, Penram International Publishing (India).
3. IBM PC and clones : Hardware , troubleshooting and maintenance, B. Govindarajalu, Tata McGRaw Hill.
4. PC/XT technical reference manual, IBM.
5. The Intel Microprocessor : 8086/8088, 80186,80286,386 and 486 - architecture, programming and interfacing 3rd edition, Barry Brey, Prentice Hall of India.
6. Advance MS-DOS , Ray Duncan, BPB publication.
7. Handbook of software and hardware interfacing for IBM-PC Jeffrey Royer, Prentice Hall of India.
8. Advanced Microprocessors and IBM-PC Assembly Language Programming, K.Udayakumar and B.S. Umashankar, Tata McGraw-Hill.

List of Experiments :

All the programs should be written in assembly language.

Group A

1. Using centronics protocol interfacing a printer to PC.
2. ADC interfacing.
3. DAC interfacing
4. Writing a program to create, write and close a file using DOS interrupts
5. Writing TSR routine.
6. PC-PC communication through serial port.
7. Stepper motor interfacing.
8. Writing device driver.

Group B

1. Interfacing LED and switches to printer port.
2. Mouse interface.
3. Read/write sectors of floppy.
4. Format a track of a floppy.
5. Read partition table of a hard disk.
6. Write graphics line editor.
   Using prototype add on card, bread board interface to operate relay, accept input, etc.
8. Study of PC motherboard and typical add on cards.

The termwork should inlcude a minimum of six experiment each from groups A and B where experiment no. 8 in both groups is compulsory.The termwork marks will be based on performance in theory and practicals with a weightage of 40% and 60% respectively.

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Term II Paper - 5
Instrumentation and Diagnostic Tools

Teaching Scheme
Lectures : 4 Hrs./Week
Practical : 2 Hrs./Week

Examination Scheme :
Paper : 100 marks
(3 Hrs. duration)
Termwork : 25 marks
Practical : 25 marks

Unit 1

Measurement and Error : Definition of instrument, accuracy, precision, sensitivity, resolution, error; Accuracy and Precision, Significant figures; Types of error, gross errors, systematic errors and random errors; Statistical analysis, arithmatic mean, deviation from the mean, average deviation, standard deviation, Probability of errors, normal distribution of errors, probable error, limiting errors. (5Hrs.)

Standards of measurement : Classification of standards, International standards, Primary standards, Secondary standards, working standards; Time and frequency standards; Eletrical standards, the absolute ampere, resistance standards, voltage standards, capacitance standards, inductance standards, standerds of temperature and illuminious intensity, IEEE standards. (5 Hrs.)

20 Marks

Unit 2

Transducers as input elements to instrumentation systems : Classification, passive and self generating types; Selecting a transducer, Strain gauges, gauge factor, application; Displacement transducers, Sensing elements, diaphragm, Bellows, Bourden tube, capacitive transducer, inductive transducer, linear variable differential transformer (LVDT); Temperature meeasurements, resistance thermometers, thermocouples, thermistor characteristics, thermistor applications; piezoelectric transducer, photoconductive cells. 20 marks. (10 Hr

Unit 3

Digital Voltmeters : General characteristics; classification, ramp-type, integrating, continuous-balance type, successive-approximation DVMs, Block diagram and working principle of each type. (5 Hrs.)

Measurements of capacitance and inductance by phase-shift method. (1 Hrs.)

Qmeter : basic Q meter circuit: measurement methods, direct connection, series connection; sources of error. (4 Hrs.)

20 Marks

Unit 4

Oscilloscopes : Block diagram and working; screens for CRTs, CRT circuits; Vertical deflection system, Delay line, Multiple trace, horizontal deflection system; Measurement of frequency, phase angle and time delay. (6 Hrs.)

Signal generators : frequency divider generator, Pulse and Square-wave generators; Function generators. (4 Hrs.)

20 marks.

Unit 5

Signal analyzers : Fundamental suppression harmonic distortion analyzer; spectrum analyzer, applications (3 Hrs.)

Data acquisition systems : Instrumentation systems; Magnetic tape recorders; D/A conversion, A/D conversion, Multiplexing, D/A and A/D. (7 Hrs.)

20 marks

References :

1 Electronic Instrumentation and Measurement Techniques, 3rd edition, W.D. Cooper and A.D. Helfrick, Prentice-Hall of India.

2 Instrumentation - Devices and Systems, 2nd edition, Rangan, Sarma and Mani, Tata McGraw-Hill.

List of Experiments :

1 Characteristic of LVDT.
2. Study of digital Voltmeter.
3 Measurement of capacitance by phase-shift method.
4 Measurement of inductance by phase-shift method.
5. Measurement of L,C,R and Q by Q-meter.
6. Study of C.R.O.
7 Measurement of distortion by distortion-factor meter for sine, square and traingular waves.
8 Measurement of square-wave responce of low-pass and high-pass RC circuits with the help of CRO.
9 Application of resistance thermometer.
10. Application of capacitive transducer for level measrement.
11 Study of Spectrum analyzer
12. Study of Data acquisition system.

The termwork should include a minimum of eight experiments from the above list. The termwork marks will be based on performance in theory and practicals with a weightage of 40% and 60% respectively.

Term-II (Paper-6)

Practical Training/ Special Study/Minor Project

(Common with TE (Electronics, Industrial Electronics, Electronic and Telecommunication Engineering & Computer Engg., Electrical Engg., Instrumentation, Mech., & Production Engg.)

Examination scheme :
Termwork : 25 marks

Every student need to complete following requirements for termwork of Practical Training/Special Study/ Minor Project.

Practical training in any industry for a period of minimum two weeks and submit training report certified by personnel manager or works manager or any other higher authority of that industry.

OR

Special study on a recent topic from reported literature and submit a report on it.

OR

Mini theoritical or fabrication project and submit a report on it.

OR

Attend a course of Entrepreneurship Development course conducted by college and submit a report on it.

NOTE:-

1. Practical training is to be undergone in Summer Vacation after S.E. and / or in Winter Vacation after first term of T.E.
2. Report should be typed on A-4 size paper and three copies paper bounded are to be prepared, one copy is for the candidate, one for the library and one for the teacher concerned.

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