NORTH MAHARASHTRA UNIVERSITY, JALGAON (M.S.)

SYLLABUS

MASTER OF ENGINEERING (M.E.)

(VLSI & EMBEDDED SYSTEM DESIGN)

2011-2012

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year (First Semester)

Sr. No.	Subject	Teaching Scheme Hours/Week		Examination Scheme				
					Maximum Marks			
		Lectures	Practical	Paper Duration Hours	Paper	Term Work	Practical	Oral
1	Microprocessor & Microcontroller Interfacing	3	-	3	100	-	-	-
2	Embedded System Design	3	-	3	100	-	-	-
3	Digital VLSI Design	3	-	3	100	-	-	-
4	VLSI Testing & Verification	3	-	3	100	-	-	-
5	Elective – I	3	-	3	100	-	-	-
6	Laboratory Practice-I	-	6	-		100	-	50
7	Seminar-I	-	4	-		100	-	-
	Total	**15**	**10**	-	**500**	**200**	-	**50**
	Grand Total	**25**			**750**			

Elective I:

1. Advanced Digital Signal Processing
2. Computer Networks & Management
3. Artificial Neural Networks & Fuzzy Systems
4. Wireless Communication System

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year (Second Semester)

Sr. No.	Subject	Teaching Scheme Hours/Week		Examination Scheme				
					Maximum Marks			
		Lectures	Practical	Paper Duration Hours	Paper	Term Work	Practical	Oral
1	Real Time Operating System	3	-	3	100	-	-	-
2	Embedded Networking & Wireless Sensor Networks	3	-	3	100	-	-	-
3	Analog VLSI Design	3	-	3	100	-	-	-
4	Nano Electronics	3	-	3	100	-	-	-
5	Elective – II	3	-	3	100	-	-	-
6	Laboratory Practice-II	-	6	-		100	-	50
7	Seminar-II	-	4	-		100	-	-
	Total	**15**	**10**	-	**500**	**200**	-	**50**
	Grand Total	**25**			**750**			

Elective II:

1. Image and Video Processing
2. Electromagnetic Interference & Compatibility
3. FPGA Based System Design
4. RF Circuit Design

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year (First Semester)

Sr. No.	Subject	Teaching Scheme Hours/Week		Examination Scheme				
					Maximum Marks			
		Lectures	Practical	Paper Duration Hours	Paper	Term Work	Practical	Oral
1	Seminar –III	-	4	-	-	50	-	50
2	Project Stage – I	-	18	-	-	100	-	-
	Total	22			200			

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year (Second Semester)

Sr. No.	Subject	Teaching Scheme Hours/Week		Examination Scheme				
					Maximum Marks			
		Lectures	Practical	Paper Duration Hours	Paper	Term Work	Practical	Oral
1	Progress Seminar	-	-	-	-	50	-	-
2	Project Stage – II	-	18	-	-	150	-	100
	Total	18			300			

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

MICROPROCESSOR & MICROCONTROLLER INTERFACING

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: MICROPROCESSOR ARCHITECTURE

Intel 386EX: *Instruction set – Data formats – Instruction formats – Addressing modes – Memory Hierarchy – Register file – Cache – Virtual memory and paging – Segmentation – Pipelining.* The instruction pipeline, Pipeline hazards, Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC, RISC properties, RISC evaluation – On-chip register files versus cache evaluation. (Ref. T1, T6).

Unit 2: HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

The software model – functional description – CPU Pin descriptions – RISC concepts – bus operations – Super scalar architecture – Pipelining – Branch Prediction – The instruction and caches – Floating point unit – Protected mode operation – Segmentation – paging, Protection, multitasking, Exception and interrupts, Input/Output – Virtual 8086 model – Interrupt processing – Instruction types – Addressing modes – Processor flags – Instruction set – Basic programming the Pentium Processor. (Ref. T1, T7).

Unit 3: 16 Bit MICROCONTROLLER (PIC)

Introduction to PIC microcontroller, *PIC16F84A -hardware architecture*, 16 Bit Instructions set of PIC16F84A, Programming of PIC16 microcontroller using assembly language, PIC18F452 microcontroller architecture, Programming of PIC18F452 using C, Development tools Like MPLAB. PIC18: *Interrupt, resets, configuration, parallel ports, Timers and CCP modules, Addressable USART, SPI, I^2C, CAN bus, Watch dog timer, ADC, DAC interface, Case studies in C language.* (Ref. T2, T3).

Unit 4: 32 Bit MICROCONTROLLER

ARM Family, ARM-7TDMI introduction, ARM7TDMI: *Programming model, Memory interface, instruction cycle timing, signal description, introduction to ARM instruction set, Thumb instruction set, Memory management unit memory protection, Case studies of Arm7.* Introduction to Features of ARM9 & ARM CORTEX M3, ARM9: *Exception handling in ARM, Interrupts, ARM procedure call Standards (APCS), ARM Thumb Interlocking. Memory mapping and data mapping in ARM, C and Assembly Interfacing, Advantages over ARM7.* (Ref. T4, T5).

Unit 5: INTERFACING TO MICROCONTROLLERS

Input devices interfacing to PIC16F877 (Keypad, Keyboard, Sensors etc.), Output devices interfacing to PIC16F877 (LCD display, printers, monitors, graphical display etc), PIC18: *CAN interface, USB interface, In-Cicuit debugging, Real Time clock interfacing, Low power RF circuit interface with Programming.* (Ref. T2, T3, and T8).

Textbooks:

T1. Barry B. Brey, "The Intel Microprocessors Architecture, Programming and Interfacing" Prentice Hall of India, 2002.

T2. Huang, PIC Microcontroller: an Introduction to software & Hardware interfacing, Thomson-Delmer Learning.

T3. Bates, Smith, Martin, Hellbuyck- PIC microcontrollers: know it all, Newnes.

T4. Joseph Yiu, The Definitive guide to the ARM Cortex M3, Newnes.

T5. ARM7TDMI Technical Ref.ence Manual.

T6. Intel 386EX User Manual.

T7. Gene. H.Miller, "Micro Computer Engineering", Pearson Education, 2003

T8. John.B. Peatman, "Design with PIC Micro controller", Pearson Education, 2003.

References:

R1. Steave Furber, "ARM System – On – Chip Architecture" Addison Wesley, 2000.

R2. David Calcutt, Fred Cowan, and Hassan Parchizadeh, "8081 Microcontrollers" An imprint of Elsevier, 2006.

R3. Andrew N Sloss, Dominic Symes, Chris Wright "ARM System Developers Guide-Designing and Optimizing System software", Morgan Kaufmann Publishers, 2004

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

EMBEDDED SYSTEM DESIGN

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: BASIC CONCEPT & ARCHITECTURE OF EMBEDDED SYSTEM

Introduction to Embedded System, History of Embedded System, Classification of Embedded System, Major Application Areas of Embedded System, Embedded System Vs General Computing System, Specialties of Embedded System, Software Tools for Embedded System, Hardware Tools for Embedded System. Example of Embedded Systems, Recent Trends in Embedded System, Design Challenge – Optimizing Design Metrics, Processor Technology, IC Technology, Design Technology, Trade-offs. **Architecture of Embedded System:** Custom Single Purpose Processor: Hardware, Combinational Logic, Sequential logic, Custom Single Purpose Processor Design, RT-Level Custom Single Purpose Processor Design, Optimizing Custom Single Purpose Processor, General Purpose Processor: Software, Basic Architecture, Operation, Programmer's View- Instruction Set, Program and Data Memory Space, Registers, I/O, Interrupts, Integrated Development Environment(IDE), Application Specific Instruction Set Processor (Ref. T1).

Unit 2: PROGRAMMING FOR EMBEDDED SYSTEMS

Overview of ANSI C, GNU Development Tools Chain, Bit manipulation using C, Memory Management, Timing of Programs, Device Drivers, Types of Device Driver , Productivity Tools, Code Optimization, Coding Guidelines, Programming in C. (Ref. T2, T5).

Unit 3: EMBEDDED SOFTWARE ISSUES

Interrupt basics, the shared data problems, interrupt latency, round robin, Round Robin with interrupt, function, Semaphore, Queue, Scheduling architecture, RTOS architecture, Message Queue, MailBox, Pipes, Timer functions, Encapsulating Semaphores & Queues, Hard real time scheduling consideration, Saving memory space, Saving power. (Ref. T6).

Unit 4: EMBEDDED SYSTEM DEVELOPMENT LIFE CYCLE

Problem Statement, Embedded Solution Hardware: Requirement Specification, Chipset selection, Schematic Diagrams, PCB layout, PCB Assembly, Board Bring-up, Software: The Development Process, Requirement specification, Plan , Tool selection, low and high level Design, Implementation, Integration of module, Integration with Hardware, Debugging and Testing, Product packaging, Certification, Type of Certification, Packaging. (Ref. T2, T3 and T5).

Unit 5: INTRODUCTION TO RTOS

Need of Real time system & RTOS, Difference between RTOS & OS, Foreground and background systems & Execution, Critical Section of Code, File structure, Kernel, Static and Dynamic Priorities. Priority inversion, Mutual exclusion, Interrupts: *advantages & disadvantage*, scheduler, Synchronizing tasks, ISRs, Inter task communication mechanism. (Ref. T2, T4).

Textbooks:

T1. Frank Vahid and Tony Givargies, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley and Sons.

T2. Dr. K. V. K. K. Prasad, “Embedded/ Real Time System”, Dreamtech.

T3. Shibu K .V. “Introduction to Embedded Systems”, Tata McGraw Hill.

T4. Iyer & Gupta, “Embedded Real Time Programming”, Tata McGraw Hill.

T5. Rajkamal, “Embedded Systems”, Tata McGraw Hill.

T6. Simon David, “Embedded Software Primer”, Pearson Education.

References:

R1. Arnold Berger, Arnold H. Berger **“**Embedded systems design: an introduction to processes, tools, and techniques”, CMP Books.

R2. Steve Heath, “Embedded System Design”, Newnes.

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First Year Term – I

DIGITAL VLSI DESIGN

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: VHDL

Introduction to VHDL, Types of modeling, Functions, Procedures, Attributes, Packages & Configurations, Synthesizable & Non Synthesizable VHDL Statements, Test benches, Modeling of digital circuits in VHDL. High Level Synthesis, Logic Synthesis, Logic Optimization, Timing optimization, Technology mapping. (Ref. T3,T5).

Unit 2: STATE MACHINES

Introduction to sequential circuits, Design and analysis of sequential circuits, Metastability synchronization, Design & Analysis of clocked synchronous sequential network. ASM chart, ASM Realization, Design of finite state machines, State machine diagram, State machine applications, State minimization, state Encoding techniques, VHDL coding of FSM, Synchronizing Glitch Free state machines, FSM state studies. (Ref. T3, T4).

Unit 3: FPGA

Introduction to FPGA, Study of architecture of FPGA, Characteristics of FPGA, FPGA Fabrics, Selection criteria of FPGA for digital design, Study of Xilinx & Altera FPGAs (Spartan 3 XC3S500, Virtex XCV 800, Cyclone EP1C20 etc.) : *Features, Block diagram explanation, Applications*. Advantages of FPGA Design, Applications of FPGA, and FPGA Design flow. (Ref. T3, T7, and T8).

Unit 4: CPLD

Introduction to CPLD, Study of architecture of CPLD, Selection criteria of CPLD, for digital design, Study of Xilinx Coolrunner XC2C256 , Altera MAX7000 EPM7256B, CPLD Architecture. In circuit programming, Design Security, Power consumption issues, Advantages of CPLD Design, Applications of CPLD, CPLD design flow. (Ref. T9, T10).

Unit 5: SEMICONDUCTOR MEMORIES

Basics of memories, Types of memory cell & memory architecture, Types of memory based on architecture, Basics of memories, Types of memory cell, SRAM, Low power SRAM technology, DRAM, SDRAM, RDRAM, FLASH, FIFO, Pseudo Static RAM, OTP ROM, Cache Mapping Techniques, Cache replacement policy, Cache write techniques, Advanced RAM, Low voltage low power memories, Memory modeling using VHDL. (Ref. T1, T2, and T6).

Textbooks:

T1. David A Hodges, “Semiconductor memories” IEEE Press.

T2. Betty Prince, “Semiconductor memories: a handbook of design, manufacture and application”, Wiley.

T3. Stephin Brown, Zwonko Vranesic, “Fundamentals of digital logic with VHDL Design”, McGraw Hill.

T4. William I. Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India, 1996.

T5. Douglas Perry, “VHDL”, McGraw Hill.

T6. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI Design” Wiley.

T7. Cyclone Device Handbook, Altera Inc.

T8. Virtex Handbook, Xilinx Inc.

T9. Xilinx Manuals.

T10. Altera Manuals.

References:

R1. James E. Palmer, David E. Perlman, "Introduction to Digital Systems", Tata McGraw Hill, 1996.

R2. N. N. Biswas, "Logic Design Theory ", Prentice Hall of India, 1993.

R3. S. Devadas, A. Ghosh and K. Keutzer, " Logic Synthesis ", Mc Graw Hill, 1994.

R4. Charles H. Roth , “Fundamentals of Logic design” Thomson Learning, 2004.

R5. Nripendra N Biswas, “Logic Design Theory” Prentice Hall of India, 2001.

R6. Parag K Lala, “Digital System design using PLD” BS Publications, 2003.

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

VLSI TESTING & VERIFICATION

Teaching Scheme:
Lectures: 3 Hrs / week

Examination Scheme:
Theory Paper: 100 Marks (3 Hours)

Unit 1: ASIC

ASIC Design Flow, Types of ASICs, Library Cell design, Library Architecture, Gate Array Design, Standard Cell Design, Datapath Cell Design, Programmable ASIC logic cells: *Actel ACT 205, Xilinx LCA 218, Altera Flex 223*, ASIC Construction: *Physical Design, CAD tools, System Partitioning, Estimating ASIC Size, Power Dissipation, Partitioning Methods*, Floor planning of ASIC, Placement & Routing. (Ref. T3).

Unit 2: SIMULATION & VERIFICATION

Fundamentals of Simulation, Types of Simulation, Logic Simulation models, Logic Simulation techniques, Simulation of VLSI interconnects, Functional verification numerical methods of transient analysis, Simulation of non linear devices, Static timing analysis, VITAL in VHDL, Design automation & verification. (Ref. T3, T6, and T7).

Unit 3: DESIGN FOR TESTABILITY

Need for DFT, Introduction to fault coverage, Testability, Design for Testability, Contrallability, Observability, Logic built in self test, Test compression, Stuck at fault model, Stuck open and stuck short faults, Scan design, BIST, Boundary Scan check, JTAG technology, Scan path, Full & partial scan, Fault simulation & Test generation, ATPG. (Ref. T2, T3, and T6).

Unit 4: CHIP DESIGN ISSUES

Digital layout, Analog layout, Parasitics, Matching, Noise issues, layout verification : LVS, DRC, ERC SRC, One two phase clock, Clock distribution, Power distribution, Power optimization, Design validation, Global routing, switch box routing, I/O architecture, wire parasitics, Packaging, Signal integrity. (Ref. T1, T3, and T4).

Unit 5: SYSTEM ON CHIP

SoC design methodology, Parameterized Systems on a Chip, System on Chip Peripheral cover. Soc & interconnect centric architectures, Design of SoC, Robust low voltage memory circuits, Low voltage Low power High speed I/O. (Ref. T2,T4).

Textbooks:

T1. Christopher saint /Judy saint, “IC mask design: essential layout techniques”, McGraw Hill.

T2. Ricardo Reis, Jochen A. G. Jesi, “Design of system on chip: Devices & Components”. Kluwer academic publication.

T3. M.J.S. Smith, “Application specific integrated circuits”, Pearson education.

T4. Wane Wolf, “Modern VLSI Design”, Pearson Education.

T5. Ricardo Reis, Jochen A.G.Jess, “Design of System on Chip: Devices & Components”, Kluwer Academic Publisher.

T6. Leung Terng Wang, Yao-Wen Chang, Kwang-Ting Chens, “Electronic Design Automation: Synthesis, Verification & Test”, Morgan Kaufmann Publishers.

7. Douglas Perry, “VHDL”, McGraw Hill.

References

R1. Gelyer, Allen, Strider, “VLSI Design techniques for analog & digital circuits”, McGraw Hill.

R2. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A circuits and Systems perspective”, Pearson Education.

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

Elective-I

1) ADVANCED DIGITAL SIGNAL PROCESSING

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: INTRODUCTION TO TRANSFORMS

Discrete time signal and systems, Its representation, Types of discrete time system, DFT, IDFT, FFT (DIF and DIT), Wavelet Transform. Power spectral estimation - *parametric and nonparametric method for power spectral estimation, minimum variance*. (Ref. T1).

Unit 2: FILTER REALIZATION

FIR and IIR filter. Design of digital filters-symmetric and anti-symmetric, Linear phase, optimum, Equi-ripple, FIR differentiation, Hilbert's transformers. Design of FIR filters using different Window technique.

Design of IIR filters-impulse invariance, Bi-linear transformation, Matched transformation, Frequency transformation in analog and digital domain. FIR Chips, Direct Design in Z-Plane, Mapping of Analog Transfer Functions, Mapping of Analog Filter Structures, Wave Digital Filters, Reference Filters, Wave Descriptions, Transmission Lines, Transmission Line Filters, Wave Flow building Blocks, Design of Wave Digital Filters, Ladder Wave Digital Filters, Lattice Wave Digital Filters, Bi-reciprocal Lattice Wave Digital Filters. (Ref. T1,T3).

Unit 3: ADAPTIVE FILTERS

Least mean square Adaptive filter: Overview of the structure, Operation of the LMS algorithm, LMS adaptive algorithm, Statistical LMS theory, Comparison of the LMS algorithm with the steepest Descent algorithm, Computer experiment on adaptive prediction, Computer experiment on adaptive equalization, Computer experiment on a minimum- variance distortion less response beam former, Directionality of convergence of the LMS algorithm for Nonwhite Inputs, Robustness of the LMS filter, Upper bound on the step size Parameters for Different Scenarios, Transfer function approach for deterministic input summary problems. (Ref. T2).

Unit 4: DSP ARCHITECTURE & SYNTHESIS OF DSP ARCHITECTURES

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and Multicomputer, Systolic and wave front arrays, Shared Memory architectures, Mapping of DSP Algorithms on to hardware - Implementation based on complex PEs - Shared Memory architecture with Bit – serial PEs. (Ref. T3).

Unit 5: ARITHMATIC UNITS AND IC DESIGN

Conventional number system, Redundant number system, Residue number system Bit parallel and bit serial arithmetic, Basic shift Accumulator, Reducing the memory size, Complex multipliers, Improved shift accumulator layout of VLSI circuit, FFT processor: *Specification*, *System Design Phase*, DCT processor: *Specification*, *System Design Phase*, and Interpolator as case studies (Ref. T3).

Text Books:

T1. John Proakis, Digital Signal Processing Prentice Hall.

T2. Simon Hykin, “Adaptive Filter Theory”, Pearson Education.

T3. Lars Wanhammer, “DSP Integrated Circuts”, Academic Press.

References:

R1. A.V.Oppenhiem & R.W.Schafer, Digital Signal Processing”, Prentice Hall.

R2. L.R.Rabiner & B.Gold, “Theory & application of digital signal processing”, Prentice Hall .

R3. A. Antiniou, “Digital Filters; analysis, design & application”, McGraw Hill .

R4. Salivahanan, vallavaraj ,gnanapriya, “Digital Signal Processing”, TMH.

R5. S.K.Mitra, “Digital Signal Processing”, TMH.

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First Year Term – I

Elective-I

2) COMPUTER NETWORKS & MANAGEMENT

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: MANAGEMENT PLATFORMS

The Well designed Platform system, Methods and tools, Standards and platform building blocks Management of Personal communication systems Managing Mobile Networks from cellular to satellite networks, Digital and analogue microwave radio systems: System protection, FM analogue microwave radio, Digital microwave radio - *transceiver, low capacity & high capacity*. (Ref. T1, T2).

Unit 2: TELECOM NETWORKS

Introduction, Analog Networks, Integrated Digital Networks, Integrated services Digital Networks, Cellular radio Networks, Intelligent Networks, Private Networks, Numbering, National Schemes, International Numbering, Numbering Plan for the ISDN , Public Data Networks, Charging, Routing, General, Automatic alternative routing, Numbering, Network Management, IN, VPN, B-ISDN Telecommunications Network, Management. (Ref. T3, T4).

Unit 3: TRAFFIC ENGINEERING

Network Traffic Load and Parameters Grade of Service and Blocking Probability, Modeling switching Systems, Incoming Traffic and Service Time Characterizations, Blocking Models and Loss Estimates, Delay Systems, Traffic Measurement, Lost call System, Queuing System. (Ref. T3, T4).

Unit 4: SYMMETRIC CIPHERS

Overview of network security and cryptography, model for network security, classical encryption techniques, block ciphers and data encryption standard (DES), Advanced encryption standard (AES), contemporary symmetric ciphers, and confidentiality using symmetric encryption. (Ref. T5).

Unit 5: PUBLIC KEY CRYPTOGRAPHY

RSA, key management, Different Hellman key exchange, elliptic curve Arithmetic, elliptic curve cryptography. **Message Authentication and Hash functions:** Authentication requirements, authentication functions, message authentication codes, Hash functions, security of Hash functions and MACs. **Hash Algorithms:**MD5 message Digest Algorithm, Secure Hash Algorithm, Digital Signatures and authentication protocols, Digital signature standard. (Ref. T5).

Textbooks:

T1. Salah Aidarous, Thomas Plevyak, “Telecommunications Network Management: Technologies & Implementation”, IEEE Communication Society.

T2. Wayne Tomasi, —Introduction to Telecommunication Voice Data Internet, PHI.

T3. J. E. Flood, —Telecommunication Switching Traffic and Network, Pearson Education.

T4. Viswanathan, —Telecommunication Switching Systems and Networks, PHI.

T5. William Stallings, “Cryptography” McGraw Hill.

References:

R1. Robert G. Winch, “Telecommunication Transmission Systems”, MGH.

R2. William C. Y. Lee, “Mobile Cellular Telecommunication”, MGH.

R3. John C. Bella, “Digital Telephony”, John Wiley & Sons.

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

Elective-I

3) ARTIFICIAL NEURAL NETWORK & FUZZY SYSTEMS

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: FUNDAMENTALS OF NEURAL NETWORKS AND BACK PROPAGATION NETWORKS

Basic concepts, Model of artificial neural network, Neural network architectures, Characteristics of neural networks, Learning methods, Taxonomy of Neural Network Architectures, Architecture of back propagation network, Back propagation learning, Selection of various parameters in BPN, Variations of Standard Back propagation algorithm, Associative memory. (Ref. T1).

Unit 2: CLASSIFIERS AND EVOLUTIONARY ALGORITHMS

Classifiers based on Bay's decision theory, Bayesian classification for normal distribution, Baysian inference, Estimation of unknown probability distribution, Bay's error, Linear classifiers, Linear discriminant Functions and decision hyper planes. The perceptron algorithm, Support vector machine(SVM),Separable and non separable classes, An introduction to non linear classifiers, The XOR problem, The two layer Perceptron and Radial Basis Function(RBF) network, Context dependent classification.

Genetic algorithm, Cycle of genetic algorithm, Crossover, mutation, Fitness function, Schema, Fundamental theorem of GA(schema theorem), Differential evolution(DE), Modified differential evolution(Mo DE), Multi objective optimization using evolutionary algorithms, Hybridization with clustering, Genetic programming (Ref. T1,T3, T5).

Unit 3: FUZZY SETS, RULES & REASONING

Classical sets, Fuzzy sets, Basic fuzzy properties and operations, Fuzzy relations, Fuzzy tolerance and equivalence relations, Membership functions, Fuzzy arithmetic, Numbers and vectors, Extension principle, Fuzzy If-Then rules, Fuzzy reasoning (Ref. T1,T4).

Unit 4: FUZZY INFERENCE AND DECISION MAKING

Natural language, Linguistic hedges, Rule based systems Candrical rule forms, Decomposition of compound rules, Likelihood and truth quantification, Aggregation of fuzzy rules, Fuzzy synthetic evaluation, PRef.encess and consequences, Multi objective decision making. (Ref. T1, T4).

Unit 5: AI AND SOFT COMPUTING, HYBRID SYSTEMS AND APPLICATIONS

Introduction to Artificial Intelligence, Soft Computing Constituents and Conventional Artificial Intelligence, Neuro-Fuzzy and Soft Computing Characteristics, Hybrid systems, Neuro-Fuzzy hybrids, Application of neural network and fuzzy logic in image processing and pattern recognition. (Ref. T1, T2, T3, T6).

Textbooks:

T1. Timothy J Ross, ”Fuzzy logic with engineering applications”, TMH.

T2. J. S. R. Jang, C. T. Sun, E. Mizutani, ”Neuro- Fuzzy and Soft Computing: A Computational Approach to Learning and Machine Intelligence”, PHI.

T3. S. Rajasekaran, G. A. Vijayalakshmi Pai, ”Neural Networks, Fuzzy logic, and Genetic Algorithms”, PHI .

T4. George J Klir, Bo Yuan, ”Fuzzy sets and fuzzy logic”, PHI .

T5. Simon Haykin, ”Neural Networks”, Pearson Education .

T6. Dan W. Patterson, ”Introduction to A.I. & Expert Systems”, PHI .

References:

R1. Nils J. Nilsson, “Artificial Intelligence: A new synthesis”, Harcourt Asia PTE Ltd, Morgan Kaufmann.

R2. Duda and Hart, “Pattern Recognition”, Willy Publication.

R3. Bart Kasko, “Fuzzy Engineering”, PHI .

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

Elective-I

4) WIRELESS COMMUNICATION SYSTEM

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: REVIEW OF WIRELESS NETWORKS

2G, 3G wireless networks, WLL, Cellular Concept (Ref. T2, T4).

Unit 2: MOBILE RADIO PROPAGATION

Large Scale Path Loss: Introduction to Radio Wave propagation, Free Space propagation model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering, Practical Link Budget Design Using Path Loss Models, Outdoor Propagation Models, Indoor Propagation Models, Signal Penetration into Buildings, Ray Tracing And Site Specific Modeling

Small Scale Fading and Multipath : Small-Scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Models for Multipath Fading Channels, Theory of Multipath shape factor for small- Scale Fading wireless Channels (Ref. T2,T3,T5).

Unit 3: MULTI ACCESS TECHNIQUE FOR WIRELESS COMMUNICATION

Introduction to Frequency Division multiple Access (FDMA), Time Division Multiple Access (TDMA) Spread Spectrum Multiple Access, Space Division Multiple Access (SDMA) Packet Radio, Capacity of cellular Systems. (Ref. T4,T5).

Unit 4: WIRELESS NETWORKING

Introduction to wireless Networks, Difference Between Wireless and Fixed Telephone Networks, Development of Wireless Networks, Fixed Network Transmission Hierarchy, Traffic Routing in Wireless Networks, Wireless Data Services, Common Channel Signaling (CCS), Integrated services Digital networks (ISDN), Signaling System No. 7 (SS7), An Example of SS7-Global Cellular Network Interoperability, Personal Communication services / Networks (PCS/PCNs), protocols for Network Access, Network Databases, Universal Mobile Telecommunication System (UMTS) (Ref. T1,T3).

Unit 5: WIRELESS SYSTEMS & STANDARDS

AMPS and ETACS, United States Digital Cellular (IS-54 ad IS-136) Global System for Mobile (GSM) CDMA digital Cellular Standard (IS-95), CT2 standard for cordless Telephones, Digital European Cordless Telephones (DECT) PACS- Personal Access Communication Systems, Pacific Digital Cellular (PDC), Personal Handy phone System (PHS), US PCS and ISM Bands, US wireless Cable Television, Summary Of Standards throughout the world, problems. IEEE 802.11. (Ref. T1, T3).

Textbooks:

T1. Feher, “Wireless Digital Communications”, PHI, New Delhi .
T2. W.C.Y.Lee, “Mobile Communications Engineering: Theory and Applications”, 2nd Ed, Mc Graw Hill.
T3. John Schiller, “Mobile Communications”, Pearson Education Asia Ltd.
T4. Theodore S. Rappaport, “Wireless Communications Principals & Practice”, (PH, NJ).
T5. Bernard Sklar, “Communication Systems”, Low Price Edition, Pearson Education.

Reference:

R1. Yi-Bing Lin, Imrich Chiamtac , “Wireless & Mobile Network Architecture”, John Wiley Publication.
R2. David Tse, Pramod Viswanath, “Fundamental of Wireless Communication”, Cambridge.

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M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

LABORATORY PRACTICE-I

Teaching Scheme:	**Examination Scheme:**
Practical: 6 Hrs per week	**Term Work: 100 Marks**
	Oral: 50 marks

Experiments / Assignments based on any three subject out of which one should be elective from First Year Term– I syllabus. The concerned subject in-charge should frame minimum of six laboratory experiments or assignments, two from each subject.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – I

SEMINAR-I

Teaching Scheme:	**Examination Scheme:**
Practical: 4Hrs / week	**Term Work: 100 Marks**

Seminar on related state of the art topic of student's own choice approved by the department

Term Work

The term-work and presentation of the Seminar-I will be evaluated by departmental committee consisting of guide and two faculty members of the department appointed by Director / Principal of the college as per the recommendation of the Head of the Department.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

REAL TIME OPERATING SYSTEM

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: STRUCTURE OF RTOS µCOS-II / EMBEDDED LINUX

RTOS features, Resources and shared resources Task, Task control block. Ready list, Task scheduling. Task level context switching, Syntax related to Context switching, Locking and unlocking of scheduler, Idle & Static task, Interrupt under RTOS, ISR under RTOS, Servicing an interrupt, Clock Tick. Initialization and Starting the RTOS, Multitasking, Task Management function, Event Control Blocks, Task State Management. (Ref. T1, T2, T4).

Unit 2: SYNCHRONIZATION & COMMUNICATION IN µCOS-II / EMBEDDED LINUX

Semaphore Management Functions with µCOS-II / Embedded Linux API , ECB as Semaphore, Mutual exclusion semaphore Functions, Event Flag management Functions, Mailbox management, ECB As Mailbox, Message Queue management, ECB as Message Queue, Message Queue Management Function. (Ref. T1, T2, T5).

Unit 3: MEMORY MANAGEMENT IN RTOS

Memory Management, Memory Control Block, Dynamic memory allocation. (Ref. T1).

Unit 4: INTRODUCTION WinCE

Introduction WinCE, Platform Builder Installation, BSP Cloning, OS Design, Catalog View & Solution Explorer, Explanation of Application, Kernel, OAL, Explanation of CPU, SoC, Platform, MMU, MMU for ARM based devices in WinCE, Overview of Boot loader, Eboot Directory Structure, Implementing Startup Code. Comparison study of µCos-II, Embedded Linux, RTLinux, Vx-works, QNX Nutrino, ThreadEX (Ref. T2, T5).

Unit 5: REAL LIFE / INDUSTRIAL EXAMPLES

Case studies examples like embedded system using RTOS for Washing Machine, Air Conditioner, Microwave Oven, Engine Management System using CAN (Maruti Swift), Automatic Chocolate Vending Machine (Ref. T1, T6).

Textbooks:

T1. Jean J. Labrosse, “MicroC/OS-II The Real Time System Kernel”, 2nd ed.

T2. Dr. K.V.K.K Prasad, “Embedded/Real Time Systems: Concepts, Design and Programming – The Ultimate Ref.ence”, Dreamtech Press, 2003

T3. Sriram Iyer, Pankaj Gupta, “Embedded Real time Systems Programming” , Tata McGraw Hill Publishing Company Limited, 2004.

T4. David E.Simon, “an Embedded Software Primer”, Pearson Education Asia, First Indian Reprint 2000.

T5. Samuel Phuns, “Professional Windows Embedded CE 6.0”, Wrox.

T6. Rajkamal, “Embedded System”, Tata McGraw Hill.

References:

R1. Dreamtech Software Team, “Programming for Embedded Systems”, Wiley Publishing Inc., 2003.

R2. Ahmed M Ibrahim, Fuzzy logic for Embedded Systems Applications, Newness an imprint of Elsevier, 2004.

R3. C.M. Krishna, Kang G.Shin, ‘Real Time Systems”, The McGraw Hill International Editions Computer Science Series.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

EMBEDDED NETWORKING & WIRELESS SENSOR NETWORKS

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: EMBEDDED NETWORK REQUIREMENTS

Embedded Networking, Communication Requirements, Requirement of wireless networks, Application of wire and wireless Networks, Advantages and Disadvantages of wire and wireless Networks, Comparison study of wire and wireless Network - Introduction to wire and Wireless Networking, Study of wire and wireless network application (Ref. T1).

Unit 2: EMBEDDED NETWORK PROTOCALS-CAN

Controller Area Network: CAN Overview, CAN open configuration, Selecting of CAN Controller, CAN development tools. Evaluating System requirements choosing devices and tools, Configuring single devices, Overall network configuration, Network simulation, Network Commissioning, CAN advantage and features, CAN Implementation: CAN Open Source code, Conformance test Implementation Issues Physical layer, Data types, Object dictionary, Communication Object Identifiers, Emerging objects, Node states. (Ref. T1).

Unit 3: EMBEDDED WIRELESS SENSOR NETWORK

Embedded Network Systems, Representation of signals, Signal propagation, Sensor Principles. Communication: Source Detection and Identification, Digital communications multiple source estimation and multiple access communications. Networking: Network Position and Synchronization Services. (Ref. T2, T4).

Unit 4: EMBEDDED WIRELESS NETWORK PROTOCALS

RF Protocol Architecture, Zigbee Protocol Architecture, Blue tooth Architecture, WiFi Architecture, Study and implantation code and Tool for all above protocols, Application of all above wireless networks protocols. Study of GSM, GPRS Network Protocol for Wireless Network Communication, Study of 2G, 3G and 4G wireless Network Protocols and application. Implementation of GSM and GPRS based wireless network thought AT Command and data & voice Transfer and make small application (Ref. T2, T3).

Unit 5: NETWORK MANAGEMENT

Energy management, Data Management, Articulation Mobility and Infrastructure. Nodes: Node Architecture, Data and Application, Network Data Integrity, Experimental System Design. (Ref. T2).

Textbooks:

T1. Glaf P. Feiffer, Andrew Ayre and Christian Keyold, "Embedded Networking with CAN and CAN open", Embedded System Academy 2005.

T2. Gregory Pottie and William Waiger, "Principles of embedded networked system design", Cambridge University Press, 2005.

T3. Jr.Edger H. Callaway, "Wireless sensor networks", CRC Press, 2004.

T4. Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks: Theory and Practice”, John Wiley.

References:

R1.Raghvendra, Sivalingam, Znati, “Wireless Sensor Networks”, Springer.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

ANALOG VLSI DESIGN

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: CMOS BASICS

MOS transistor theory, MOS transistor inverters, Static & Dynamic characteristics, Power consumption, Power Delay Product, CMOS Latch effects, Prevention of Latch Effect, CMOS Fabrication Processes: *nWell, pWell, Twin Tub, SOI*, CMOS layout, Transmission gate. (Ref. T6).

Unit 2: MODELING OF DEVICES

Integrated bipolar transistor, Types & structures in monolithic technologies, Basic model (Eber Moll), Gummel poon model, Dynamic model parasitic effects, SPICE model-parameter extraction. Integrated MOS transistor-Threshold voltage, Threshold voltage equations, Threshold Adjustment, MOS device equation, Basic DC equations, MOS models small signal , AC characteristics , MOS SPICE model level 1,2,3,4. (Ref. T6, T7).

Unit 3: AMPLIFIERS

Theory & Design of MOS operational amplifiers, Complete CMOS operational amplifier including frequency compensation, Stability, Frequency response and transient response . High performance CMOS Op-amp, Active & passive current mirror, Switched capacitor circuits. (Ref. T1, T2).

Unit 4: BiCMOS

Basic BiCMOS circuit techniques, BiCMOS process, Digital and analog BiCMOS Process flow ,BiCMOS inverters ,BiCMOS logic circuits. (Ref. T3, T4).

Unit 5: CONVERTERS

RF Analog Circuits & Sub circuits: Capacitors & Inductors in VLSI circuits, Bandwidth estimation techniques, Design of high frequency amplifiers, Design of low noise amplifiers, Design of Mixers of RF power amplifiers, Architectures of RF receivers and transmitters. (Ref. T5).

Textbooks:

T1. D.A.John & Ken Martin, “Analog Integrated Circuit Design”, John Wiley, 1997.

T2. Philip Allen, Douglas Holberg, "CMOS Analog Circuit Design", 2nd Ed, Oxford Press – 2002.

T3. Sung Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits”, TMH.

T4. Antonio R. Alvarez, “BiCMOS Technology and Applications”, Kluwer Academic Publisher.

T5. Behzad Razavi, “Analysis and Design of CMOS integrated Circuits”, Tata McGraw Hill, 2008.

T6. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A circuits and Systems perspective”, Pearson Education.

T7. Michel Shur, “Physics of Semiconductor Devices”, Prentice Hall.

References:

R1. Nandita Dasgupat, Amitava Dasgupta “Semiconductor Devices: Modelling and Technology”, Prentice Hall of India, 2007.

R2. Gregolian & Temes: “Analog MOS Integrated Circuits”, John Wiley, 1986.

R3. Andrew Brown, “VLSI circuits and systems in silicon”, Mc Graw Hill, 1991.

R4. Gray, Meyer, Lewis Hurst “Analysis & Design of Analog IC”, Wiley International 4th Ed. 2009.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

NANO ELECTRONICS

Teaching Scheme: **Examination Scheme:**
Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: IC FABRICATION

Crystal growth techniques, Czochralski Crystal Growth, Wafer preparation, Epitaxy: *Chemical Vapour Deposition, Molecular Beam Epitaxy*, Photolithography, Etching: *Dry and Wet*, Diffusion, Oxidation: *Dry, Wet, Thermal Oxidation*, Ion implantation, Metallization, Annealing bonding, Mask design (Ref. T2).

Unit 2: SCALING OF DEVICES

Scaling theory, Scaling of MOSFET, Advantages of scaling, Full & partial scaling, Limitation of scaling ,Technology scaling challenges, Circuit design challenges and leakage control technology, CAD related issues, High- K dielectrics ,Concept of EOT . (Ref. T3).

Unit 3: REVIEWS OF QUANTUM MECHANICS AND SOLID STATE PHYSICS

Top down and bottom up methodology ,Review of classical mechanics, De-Broglie's hypothesis, Heisenberg uncertainty principle, Pauli exclusion principle, Schrodinger's equation, Properties of wave function , Structure and bonding ,Lattice vibration ,Energy bands ,Insulators ,Semiconductors ,and conductors , Energy gap of semiconductor, Fermi surface localized particles, Donar ,Acceptors, Deep traps, Mobility and excitation. (Ref. T1, T6).

UNIT 4: NANO ELECTRONICS

Molecular electronics, Molecular switching, Schottky devices, Quantum structures and devices, Mesoscopic devices , Nanoscale transistor ,Single electron transistor, SET logic gates ,MOSFET and NanoFET ,Resonant tunneling devices, Carbon Nanotubes, Connection with quantum dots, Quantum wires ,Quantum well, Quantum dot lasers, Nanolithography-Lithography using photon and particle beams ,Scanning probe lithography, Soft lithography. (Ref. T1, T6, T7).

UNIT 5: MEMS

Introduction to MEMS, Actuation techniques, MEMS fabrication processes, RF MEM, Application of MEMS in communication. (Ref. T4, T5).

Textbooks:

T1. C.P. Poole Jr., F.J. Owens, "Introduction to Nanotechnology", Wiley (2003).

T2. M. Sze (Ed), "VLSI Technology", 2nd Ed, McGraw Hill, 2008.

T3. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A circuits and Systems perspective”, Pearson Education.

T4. Minang Bao, “Analysis and design principle of MEMS devices”, Elsevier Publication.

T5. M. Gadel-hak, “ The MEMS handbook”, CRC Press.

T6. Hanson, “Fundamentals of nanoelectronics”, Pearson Education.

T7. Edward Wolf, “Quantum Nanoelectronics: an introduction to electronics nanotechnology and Quantum Computing”, Wiley VCH.

References:

R1. John H. Davies, “The Physics of Low-Dimensional Semiconductors” Cambridge University Press, 1998.

R2. C. Y. Chang & S. M. Sze), “ULSI Technology”, 2nd Ed, McGraw Hill, 2002 Ning & Taur.

R3. Waser Ranier, “Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices)”, Wiley-VCH (2003).

R4. K.E. Drexler, “Nano Systems”, Wiley Publications (1992).

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

Elective-II

1) IMAGE AND VIDEO PROCESSING

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: INTRODUCTION TO DIGITAL IMAGE & IMAGE TRANSFORMATION

Digital Image representation, Elements of visual perception, Image model, sampling uniform and non-uniform Sampling , Quantization-uniform and non-uniform, relationship between pixels - neighbors, connectivity, distance, Imaging Geometry-Basic Transformation, Perspective Transformations, camera model, camera calibration, stereo imaging, arithmetic and logic operations on images. **Image Transformation:** overview of 1D Fourier Transform, Discrete Fourier Transform, Fast Fourier Transform, Properties of 2D Fourier transform, Fast Fourier transform, DCT, properties, Introduction to wavelet Transform continuous and discrete, properties, Other Separable Image transforms- Walsh Transform, Hadamard Transform, K L Transform, Hough Transform and properties of all. (Ref. T1, T2, T3).

Unit 2: IMAGE ENHANCEMENT

Spatial-Domain Method and Frequency-Domain Method, Histogram Modification Techniques, Local Enhancement. Spatial domain filters-Average, median, Frequency domain filter- Ideal Filters, Low pass Filtering, Butterworth Filter, High Pass filter, Ideal Filter, Butterworth Filter and Differentiation.

Image Restoration: Degradation Model, Diagonalization of Circulant and Block Circulant Matrices, Algebraic Approach to restoration, Restoration in Spatial Domain, Grey-level Interpolation. (Ref. T1, T3).

Unit 3: IMAGE COMPRESSION

Compression Fundamentals, Lossy and lossless compression, Fidelity criteria, Coding Redundancy, Encoding Process, Huffman Code, RLE, 1-D/2-D Run Length Encoding, Coding Considerations. Image standards: JPEG, JPEG2000, MPEG Standards, Various Image file formats such as - BMP, TIFF, GIF. (Ref. T1, T3, T4) .

Unit 4: IMAGE SEGMENTATION

Detection of Discontinuities, Point/Line/Edge Detection, Combined Detection, Edge Linking and Boundary Detection, Thresholding -Global/ Optimal, Region Oriented Segmentation, Basic formulation, Region growing, Region splitting and Merging. Representation and description: Representation Schemes, Descriptors, Regional descriptors, Pattern and Pattern classes, Classifiers. Image texture analysis, co-occurrence matrix, measures of textures, statistical models for textures, principal component analysis. (Ref. T1, T3).

Unit 5: PATTERNS AND PATTERN CLASSES

Recognition based on decision theoretic methods, Matching, Optimum statistical classifiers, neural networks, Structural methods: *Matching shape numbers, String matching, Syntactic*

recognition of strings, Syntactic recognition of trees. MPEG 4: *Coding of audiovisual objects, MPEG 4 systems, MPEG 4 audio and video, profiles and levels.* MPEG 7 standardization process of multimedia content description, MPEG 21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the Internet (Ref. T1, T3, T4).

Textbooks:

T1. Rafael Gonzalez and Richard E Woods, “Digital Image Processing”, Pearson Education .

T2. Arthur R. Weeks, Jr, “Fundamentals of Electronic Image Processing”, PHI .

T3. Anil K. Jain, ”Fundamentals of Digital Image Processing”, PHI.

T4. Said Ahmad, “Image Processing, Theory, Algorithm and architecture”, McGraw Hill .

References:

R1. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, “Multimedia Communication Systems”, Pearson education.

R2. Tay Vaughan, “Multimedia: Making it Work”, 6th edition, Tata McGraw Hill.

R3. K P Soman K I Ramchandran, “Insight into Wavelets from theory to practice”, 2nd Ed, PHI.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

Elective-II

2) ELECTROMAGNETIC INTERFERENCE & COMPATIBILITY

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit 1: INTRODUCTION TO EMI / EMC

Electromagnetic interference and Electromagnetic Compatibility (EMI / EMC) Standards, Introduction to E, H, Near and far field radiators, Receptors and antennas, Different types of EMI sources and possible remedies. (Ref. T1, T2).

Unit 2: MEASUREMENT TECHNIQUES IN EMI

Open Area Test Sites, Radiated interference measurements, Conducted interference measurements, Interference immunity. (Ref. T1, T2).

Unit 3: EMI REDUCTION TECHNIQUES

Grounding, Shielding, Bonding, and EMI filters. EMI Analysis and EMC Regulations: EMI Modeling, EMI analysis using Spice, EMC Regulations: FCC, VDE, MIL-STD-461, Voltage/LISN measurement method, Current /capacitor measurement method, Comparison of some of the RF conducted emission standards. (Ref. T1, T3).

Unit 4: PROBABILISTIC AND STATISTICAL PHYSICAL MODEL

Introduction to Probability considerations, Statistical Physical Models of EMI / EMC, EMC of terrestrial radio communication systems (Ref. T1,T2).

Unit 5: COMPUTER BASED MODELING AND SIMULATION

Computer Based Modeling and Simulation of EMI Models and Signal Integrity. (Ref. T1, T2, T3).

Textbooks:

T1. V. Prasad Kodali, “Engineering Electromagnetic Compatibility, Principles and Measurement Technologies”, IEEE Press-2002.

T2. Devid A. Weston, “Electromagnetic Compatibility, Principles and Applications”, Marcol Dekker, Inc New York.

T3. Jeffrey P. Mills, “EMI Reduction in Electronic Systems”, PTR PH New Jersey 2001.

References:

R1. Henry Ott, “EMI Filters and Noise Reduction Techniques”, Wiley and Sons.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

Elective-II

3) FPGA BASED SYSTEM DESIGN

Teaching Scheme: **Examination Scheme:**

Lectures: 3 Hrs / week **Theory Paper: 100 Marks (3 Hours)**

Unit: 1 FPGA ARCHITECTURE

Introduction of basic concepts, Digital design and FPGAs. FPGA based system design, Logic blocks, Routing architecture, FPGA Fabrics, Circuit design of FPGA fabrics, Platform FPGA. (Ref. T1).

Unit 2: TECHNOLOGY MAPPING FOR FPGAs

Fundamental of high level synthesis, Logic synthesis, Logic optimization and technology mapping, Lookup table technology mapping, Timing analysis, Timing optimization ,Area optimization. (Ref. T2, T5).

Unit 3: ROUTING FOR FPGAs

Routing terminology ,Strategy for routing in FPGAs ,Routing for row-logic block selection, Experimental procedure logic block architecture ,Logic block functionality vs area and efficiency ,Logic block selection ,experimental procedure logic block area and routing model. (Ref. T3, T4).

Unit 4: ARCHITECTURE OF XILINX & ALTERA FPGAs

Study of Xilinx Virtex series FPGAs, Architecture of Altera cyclone FPGA series FPGAs, Comparision of Xilinx & Altera FPGAs (Ref. T6, T7, T8).

Unit 5: APPLICATIONS OF FPGAS

Application of FPGA in digital signal processing: A detailed case study, Application of FPGA in communication system design: A detailed case study, Study of Xilinx or Altera FPGA design flow in detail. (Ref. T1, T2).

Textbooks:

T1. Wayne Wolf, “FPGA based system design”, Prentice Hall.

T2. Wayne Wolf, “Modern VLSI design, System on Chip design”, 3rd Ed. Prentice Hall.

T3. S. Trimberger, Edr, “Field Programmable Gate Array technology”, Kluwer Academic publication.

T4. Ian Kuon, Russell Tessier, Jonathan Rose, “FPGA Architecture”, Now Publishers.

T5. Rajeev Murgai, Robert King Brayton, Al Berto, “Logic Synthesis for FPGAs”, Kluwer Academic Publishers.

T6. Sparten III User Guide, Xilinx INC.

T7. Virtex II Handbook, Xilinx INC.

T8. Cyclone Device Handbook, Altera INC.

References:

R1. P.k.Chan &S .Movrad, “Digital Design using Field Programmable Gate Arrays”, Prentice Hall.

R2. John Voldfield, Richard C Dore, “Field Programmable Gate Arrays”, Wiley.

R3. www.xilinx.com.

R4. www.altera.com.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

Elective-II

4) RF CIRCUIT DESIGN

Teaching Scheme:
Lectures: 3 Hrs / week

Examination Scheme:
Theory Paper: 100 Marks (3 Hours)

Unit 1: INTRODUCTION TO RF CIRCUIT DESIGN

Overview wireless principles, Characteristics of passive IC components, Resistors, capacitors, inductors, transformers, Interconnect at RF and High frequencies skin effect complexity and choice of technology, Basic concepts in RF Design: Nonlinearity & time variance. Inter Symbol Interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion. (Ref. T1, T4).

Unit 2: RF DEVICES

BJT and MOSFET behavior of RF frequencies, Modeling of the transistors and SPICE Model, noise performance and limitations of devices, Integrated parasitic elements at high frequencies and their monolithic implementation (Ref. T4).

Unit 3: RF CIRCUITS DESIGN

Overview of RF Filter design, Matching and biasing networks, Basic blocks in RF systems and their VLSI implementation, LNA design in various technologies, Design of Mixers at GHz frequency range. Oscillators design, Resonator VCO Design, Various RF synthesizer architectures and frequency dividers, Power amplifier Design. Design issues in integrated RF filters. (Ref. T1, T2).

Unit 4: RF MODULATION

Analog and digital modulation of RF circuits, Comparison of various technologies for power efficiency. Coherent and non coherent detection, Mobile RF Communication and basics of Multiple access techniques, Receiver & transmitter architectures, Direct conversion and two step transmitters. (Ref. T1).

Unit 5: RFID TECHNOLOGY

Introduction, RFID technology, The elements in RFID system, coupling, Range and penetration, RFID application, Use of CPLDs in RFID technology. (Ref. T3).

Textbooks:

T1. B. Razavi, "RF microelectronics", Prentice Hall of India.
T2. Thomas H Lee, "Design of CMOPS RF integrated circuits", Cambridge University Press.
T3. Styeven Shepard, "Radio Frequency Identification", McGraw Hill.
T4. Ludwin, Bogdanov, "RF Circuit Design", Person Education.

Reference:

R1 E. N. Farag and M.I. Elmasry, “Mixed signal VLSI Wireless Design : Circuits and System”, Kluwer Academic.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

LABORATORY PRACTICE-II

Teaching Scheme:

Practical: 6 Hrs/week

Examination Scheme:

Term Work: 100 Marks

Oral: 50 marks

Experiments / Assignments based on any three subjects out of which one should be Elective from First Year Term – II syllabus. The concerned subject in-charge should frame minimum of six laboratory experiments or assignments, two from each subject.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

First Year Term – II

SEMINAR-II

Teaching Scheme:

Practical: 4 Hrs/week

Examination Scheme:

Term Work: 100 Marks

Seminar on related state of the art topic of student's own choice approved by the department.

Term Work

The term-work & presentation of the Seminar-II will be evaluated by departmental committee consisting of guide and two faculty members of the department appointed by Director / Principal of the college as per the recommendation of the Head of the Department.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year Term – I

SEMINAR-III

Teaching Scheme: Examination Scheme:

Practical: 4Hrs/week Term Work: 50 Marks

Oral: 50 Marks

Seminar on special topic: The topic should be on any of the area not included in the regular curriculum. The report should include detailed study of specific concept (i.e. analysis, design & implementation.). This can be a theoretical study or practical implementation approved by the department/guide.

Term Work

1. Seminar-III should be conducted at the end of Second Year Term I.

2. The term-work of the Seminar-III will be evaluated by departmental committee consisting of guide and two faculty members of the department appointed by Director / Principal of the college as per the recommendation of the Head of the Department.

3. The Seminar-III presentation will be evaluated by examiners appointed by University, one of which should be the guide.

4. Student must submit the Seminar Report in the form of soft bound copy .

5. The marks of seminar-III should be submitted at the end of Second Year Term I to the University.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year Term – I

PROJECT STAGE-I

Teaching Scheme: **Examination Scheme**:

Practical: 18 Hrs / week **Term Work:** 100 Marks

Project will consist of a system Development in Software / Hardware. Project Work should be carried out using Software Engineering principles and practices.

Term Work

The term-work of the Project Stage-I will be evaluated by departmental committee consisting of guide and two faculty members of the department appointed by Director / Principal of the college as per the recommendation of the Head of the Department.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year Term – II

PROGRESS SEMINAR

Examination Scheme:
Term Work: 50 Marks

1. Progress Seminar should be conducted in the middle of Second Year Term II.
2. The Progress Seminar Term-Work will be evaluated by departmental committee consisting of guide and two faculty members of the department appointed by Director / Principal of the college as per the recommendation of the Head of the Department.
3. Student must submit the progress report in the form of soft bound copy.
4. The marks of progress seminar should be submitted along with the marks of Project Stage II.

North Maharashtra University, Jalgaon

M.E. (VLSI & EMBEDDED SYSTEM DESIGN)

Second Year Term – II

PROJECT STAGE-II

Teaching Scheme:
Practical: 18 Hrs / week

Examination Scheme:
Term Work: 150 Marks
Oral: 100 Marks

This is in continuation of Project Stage-I. The complete System Development in software / hardware carried out using Software Engineering principles and practices is expected. It should be a working system either software or hardware or combination of both.

He / she has to present / publish at least one paper in reputed National / International Journal / Conference on his / her Project work before submission of his / her Thesis / Dissertation.

Term Work

1. The Term Work of Project Stage –II will be assessed jointly by the pair of Internal (Guide) and External examiner along with oral examination of the same**.**